# MICROCONTROLLER

UNIT-IV

Lecture-1

# MEMORY ADDRESS DECODING

- The CPU provides the address of the data desired, but it is the job of the decoding circuitry to locate the selected memory block
- Memory chips have one or more pins called CS (chip select), which must be activated for the memory's contents to be accessed
- Sometimes the chip select is also referred to as chip enable (CE)

# Contd.

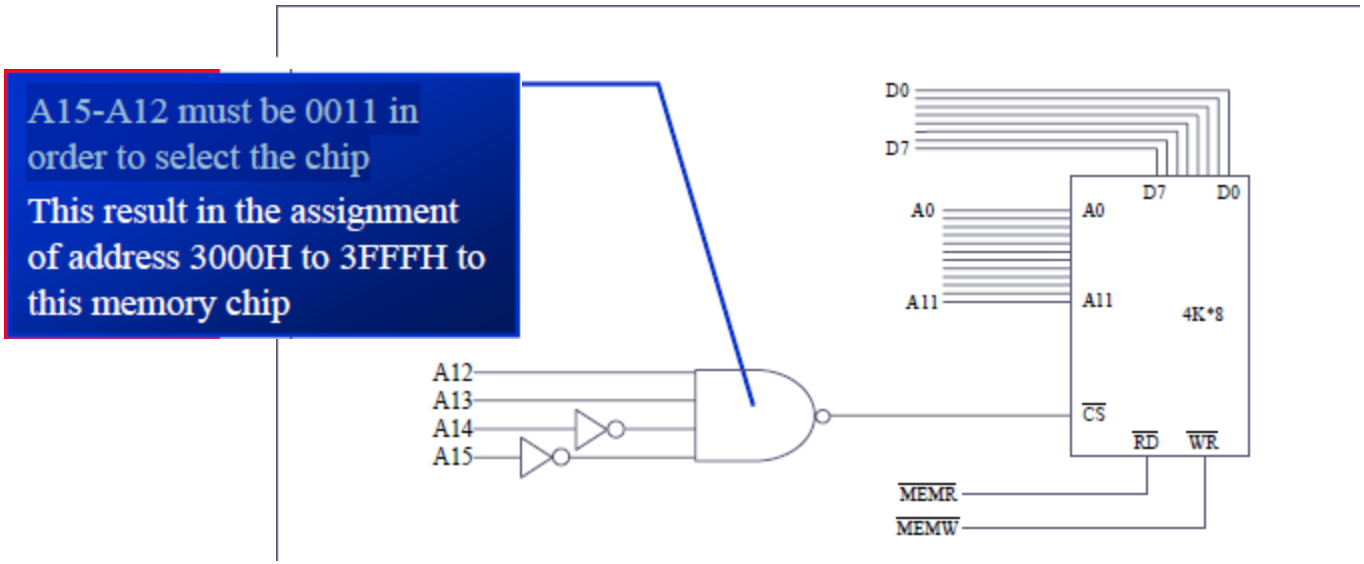
- In connecting a memory chip to the CPU, note the following points
- The data bus of the CPU is connected directly to the data pins of the memory chip
- Control signals RD (read) and WR (memory write) from the CPU are connected to the OE (output enable) and WE (write enable) pins of the memory chip

# Contd.

- In the case of the address buses, while the lower bits of the address from the CPU go directly to the memory chip address pins, the upper ones are used to activate the CS pin of the memory chip
- Normally memories are divided into blocks and the output of the decoder selects a given memory block
- Using simple logic gates
- Using the 74LS138

# Contd.

- The fact that the output of a NAND gate is active low, and that the CS pin is also active low makes them a perfect match A15-A12 must be 0011 in order to select the chip



# Contd.

- This is one of the most widely used address decoders
- The 3 inputs A, B, and C generate 8 active low outputs Y0 – Y7
- Each Y output is connected to CS of a memory chip, allowing control of 8 memory blocks by a single 74LS138
- In the 74LS138, where A, B, and C select which output is activated, there are three additional inputs, G2A, G2B, and G1

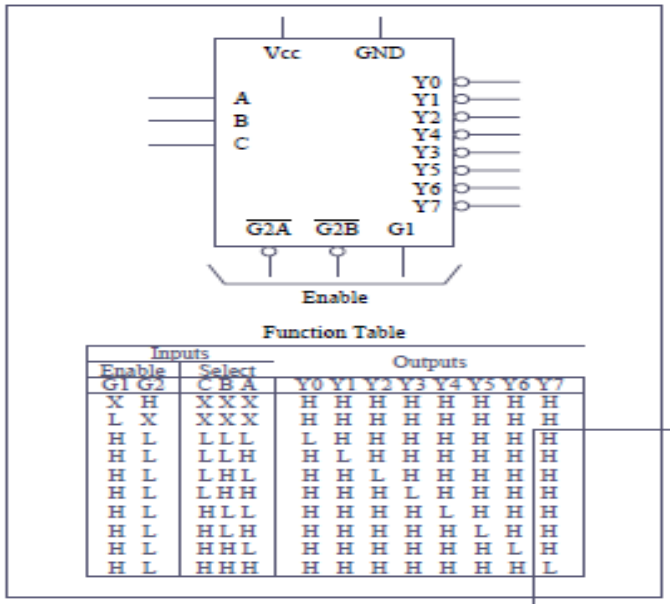
# Contd.

- G2A and G2B are both active low, and G1 is active high
- If any one of the inputs G1, G2A, or G2B is not connected to an address signal, they must be activated permanently either by Vcc or ground, depending on the activation level

Using 74LS138 3-8 Decoder

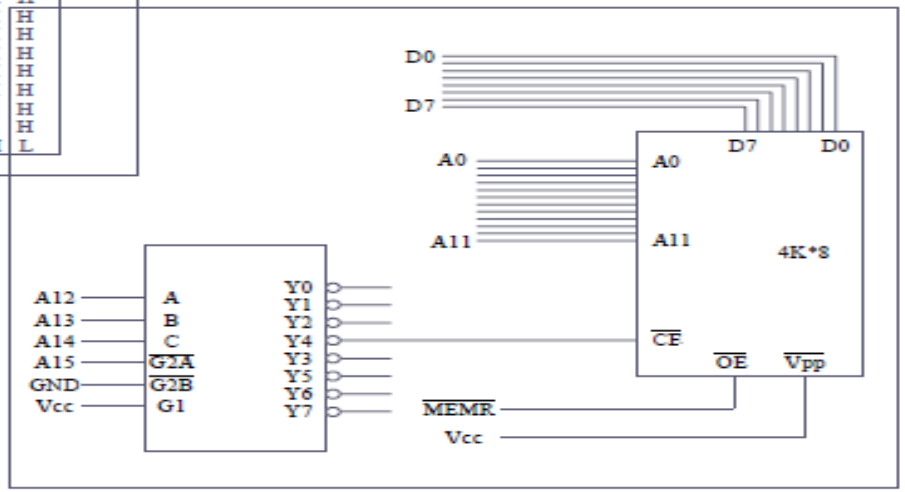
# Contd.

## 74LS138 Decoder




**Function Table**

| Inputs | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Enable | | Select | | | | | | | | | |
| G1 | G2 | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |



# Contd.

- Using programmable logics
- The simplest way of decoding circuitry is the use of NAND or other gates